

1. (Amended) A high-speed router for transmitting data packets, containing header data and useful data, between data networks, the router having a plurality of data processing processors for parallel data processing of the header data.

2. (Amended) The high-speed router as claimed in claim 1, wherein a demultiplexer is provided for separating the data packets present on the high-speed router into header data and useful data.

3. (Amended) The high-speed router as claimed in claim 1, wherein a distribution processor is provided for distributing the separated header data to the data processing processors.

4. (Amended) The high-speed router as claimed in claim 1, wherein the distribution processor distributes the header data on the basis of the priority of the header data and the workload of the data processing processors.

5. (Amended) The high-speed router as claimed in claim 1, wherein the header data are distributed to the data processing processors by means of DMA operations.

6. (Amended) The high-speed router as claimed in claim 1, wherein a CAM coprocessor having an associative memory is provided for classifying the data packets.

7. (Amended) The high-speed router as claimed in claim 1, wherein a useful data memory is provided for bufferstoring the separated useful data.

8. (Amended) The high-speed router as claimed in claim 1, wherein the header data and useful data in a data packet contain a respective identifier.

9. (Amended) The high-speed router as claimed in claim 1, wherein a first multiplexer is provided for compiling header data and useful data, the useful data coming from the useful data memory or from a switching mechanism.

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10. (Amended) The high-speed router as claimed in claim 1, wherein a second multiplexer is provided for compiling the useful data buffer-stored in the useful data memory and the header
11. (Amended) The high-speed router as claimed in claim 1, wherein the first multiplexer has a FIFO memory connected downstream of it for outputting the compiled data packets through the router.
12. (Amended) The high-speed router as claimed in claim 1, wherein the output of the second multiplexer is connected to the switching mechanism.
13. (Amended) The high-speed router as claimed in claim 1, wherein the distribution processor, the data processing processors and the CAM coprocessor are connected to a common header data bus.
14. (Amended) The high-speed router as claimed in claim 1, wherein each data processing processor is connected to a dedicated local memory.
15. (Amended) The high-speed router as claimed in claim 1, wherein a common memory is additionally connected to the header data bus.
16. (Amended) The high-speed router as claimed in claim 1, wherein the CAM coprocessor is connected to the header data bus via FIFO buffer memories.
17. (Amended) The high-speed router as claimed in claim 1, wherein the demultiplexer has an input buffer connected upstream of it.
18. (Amended) The high-speed router as claimed in claim 1, wherein the data networks are LAN networks.
19. (Amended) The high-speed router as claimed in claim 1, wherein one of the data networks is the Internet.
20. (Amended) The high-speed router as claimed in claim 1, wherein the distribution processor and the data processing processors are processors of the same processor type.

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